1.3 Towards a New Nanoelectronic Cosmology

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I. INTRODUCTION

The happy times of smooth roadmap scaling with its resulting more- or-less simple design rules, adequate supply voltage, and unimpeded circuit shrinkage, seems to be gone forever. Before the transition, we could predict circuit behaviour in a reliable manner, since we had full control of its main parameters, and we could expect economically acceptable yields: But, no longer! It all started with complex mask post-processing to extend the life of optical lithography, still further, through holographic techniques. This allowed enhanced lithography to reach submicron dimensions, with the result that the relation between expected device behaviour and real behaviour steadily increased. Then, short-channel effects and source-drain leakage became critical, and static power, previously negligible, became as important as dynamic power. To add to this already-complex context, interconnections also became a critical part of the problem. As scaling moved ahead to nanometric dimensions, devices started to change our global view of integration.

One of the results of this process of creeping deterioration is that as the sources of observable parametric variability increased, so did a mismatch between simulation results and actual measurements, at all levels. Many of these effects were already well known to analog designers. The difference is that, now. these effects are of importance even to digital design, since previous noise margins have disappeared, bringing digital designers back to the stone age!

As a result, the increased parameter-variability observed today, from one technology node to the next, tightly couples previously-thought-to-be-independent dimensions of the problem, motivating a new nano-cosmology in which global optimization results from an intricate balance between Process, Device, Circuit, Architecture, and System, technologies. Deep understanding of the underlying mechanisms is required to guide the right choices at all levels, leading to acceptable performance, manufacturability, and yield.

II. CURRENT NANOMETER CMOS TECHNOLOGIES

The evolution of CMOS through most of the scaling roadmap has been smooth, when seen in perspective, but, in fact, the enormous success of MOS, and thus of CMOS, is the result of continuous efforts in processing, with the single goal of increasing both the integration level and performance. At each successive technology node, total power was also reduced, thanks to the square law relating dynamic power to power-supply voltage. Static power, resulting from device leakage, was not an issue to the point that it was used to detect faulty devices through the IDDQ test.

More recently, as scaling started to approach the 1-to-2V power-supply level, serious concerns appeared, due to increased sub-threshold source-drain leakage currents that increased exponentially from one node to the next, as threshold voltages were reduced. This leakage problem is now aggravated by gate-oxide tunneling, a typical quantum effect. At the same time, clock frequencies approached the GHz range, and total dissipated power became the main concern, both for the computer and for the telecommunications industries, for different reasons. Packaging, chip temperature, reliability, and cost on the one side, battery life, and cost on the other.

As a result, CMOS structures, featuring new semiconductor/dielectric materials and band-gap engineering, were proposed for 45nm and beyond, and are expected to help overcome, or at least attenuate, effects related to quantum behaviour, the discreteness of matter, high-fields, mobility degradation, leakage, as well as supply-voltage scaling, under the constraint of ever-increasing system-integration levels, battery life, and performance.

Overall, system-cost pressures imply improved yields in the context of ever-increasing parameter variability, forcing new tightly-coupled system-architecture-circuit-device design techniques, imposing new challenges that will be described here:

a) Improvements in device architecture:

Today, considerable development effort is directed toward other than bulk planar (non-bulk) device-structures, since the main design show-stoppers are the increasing variations observed in threshold voltage values, and the sub-threshold leak, now aggravated by tunneling gate-leakage. Back-biasing techniques have been used for bulk devices to reduce sub-threshold leakage [1], [2].

At the present time, it is commonly admitted that the ultimate device structure will be some kind of double-gate device. Beyond the SoN (Silicon on Nothing [3]) and the original DG (Double-Gate) structure [4], many other DG structures are studied today, such as FinFET [5], OmegaFET [6], TriGate [7], Vertical [8], DeltaFET [9], Surrounding-Gate [10], etc. The electrical advantages of these structures originate in the DG operation, and thus are more-or-less independent of the fabrication mode or final geometry.

Figure 1.3.1 summarizes the evolution in device structures as proposed world-wide.

b) New metal-dielectrics gate stacks:

Gate-channel behavior can be greatly improved by increasing the dielectric barrier height, and removing the poly-gate depletion layer. The first improvement is obtained by using new gate oxides (such as, high-K, Hf-based oxides, for example), resulting in 2-to-3 orders-of-magnitude reduction of the gate-leakage current, potentially extending the use of CMOS by another 10 years to reach the 25nm node [11]. The second is achieved by the use of metal gates.

Questions related to the thermal stability and reliability of these new gate oxides need consideration, as well as, some other well-known effects such as charge-trapping, hysteresis, and Fermi-level pinning. Channel-dielectric interfaces also need revisiting, since all these effects are potential sources of carrier-mobility degradation and variability, all of these to be compared to the high standards set by SiON. Metal-gate-work-function engineering also needs a closer look, in order to improve threshold-voltage control.

c) Mobility-Enhancement Techniques:

Mobility remains a key parameter of transistor performance, but is not a source of strength for Silicon. Materials such as GaAs or InP present much higher mobilities than Si, but their technology is not compatible with that of Si VLSI. However, reasonable improvement can be expected with such Silicon-compatible materials as Ge and Strained-Si. Concerning Ge, a strong R&D effort toward SiGe epitaxial channels on Si. was carried out in the past [12]-[16].

The initial NMOS degradation observed, and the strain-relaxation with temperature, was successfully solved [16] by using a multiple-well architecture.

Many groups have now reported [18]-[21] up to a factor of 2X improvement in electron mobility (long-channel) in strained-Si (s-Si) channels on SiGe virtual substrates with around 20% Ge fraction. An example of s-Si channel implementation in an NMOS-FET is shown in Fig. 1.3.2, and the corresponding electrical char-

acteristics are given in Fig. 1.3.3. The recent interest in pure Germanium channels [17] for hole-mobility improvement, should also be noted.

Nevertheless, other techniques providing uniaxial stress were found to be much more efficient than those earlier ones providing classical biaxial stress and are now used in production. These include normal nitride layers [22], dual liners providing tensile stress, for NMOS and compressive stress for PMOS [23], or epitaxial SiGe S-D contacts for PMOS compressive-stress generation [24]. It has also recently been observed that hole mobility can be improved by using local (110)-orientation, while keeping standard (100) for NFETs [25]. If the electron-mobility enhancement is already close to its limits, the hole-mobility improvement is still increasing, leading to a global reduction in the NMOS/PMOS saturation-current ratio.

Nevertheless, one must keep in mind that the technological challenge for future CMOS nodes won't be to further increase carrier mobility, but, rather, to maintain the benefits of strain techniques in ultra-dense areas [26]

III. VARIABILITY: SOURCES AND BEHAVIORS

As CMOS approaches the 45nm node, the discrete nature of semiconductor phenomena, and the resulting stochastic behavior begins to manifest itself in many ways. This, together with added process complexity at all levels, including lithography (including Optical-Proximity-Correction (OPC) and Reticle-Enhancement Technologies), and the ever-present short-channel effects, make it increasingly difficult for designers to predict the behavior and yield of their circuit. Defects resulting from OPC include pinching, bridging, local performance-degradation, etc.

Observed variations can be either systematic (lithography and associated etching effects, implant doses, layer thickness, etc), or completely random (impurity ions under the channel, line or surface roughness, etc). Systematic variations can, in principle, be corrected by appropriate process modifications, while random variations cannot be corrected, and can only be compensated in some cases by active sensing and adaptation at the circuit level. The result is the increasing consciousness, in the micro/nano electronics community, that joint engineering is needed to move forward, taking into account all the dimensions of the problem, namely, System, Circuit, Device and Process:

a) Lithography and Proximity Effects

Thus lithography is an important source of variability because of the different ways the original design, as imagined by the designer or generated by automatic synthesis, will fail to translate into the desired device shapes. Possible sources of difference include, in addition to those mentioned above, effects deriving from the interaction between light and the photo-resist, development, and optics of the projection system, in particular, the mechanical details of the sweeping of the slit and associated optical aberrations [27]. In fact, the final features of a device and its dimensional dispersions are a complex function of its geometrical environment. Figure 1.3.4 shows the effect of dummy polysilicon lines close to the transistors of a ring oscillator on propagation delays. Similar variations are observed when the test structures are rotated by 90 degrees.

These effects are difficult to model, and electrical simulators like SPICE and the like do not include these geometrical notions. Simple corner-lot parameter variations are intrinsically pessimistic, and will not represent real parameter correlation.

b) New materials, stress- and CMP-induced variability

Stress is being used to enhance carrier mobilities, through the deposition of appropriate SiGe (or SiC) epitaxial layers, as source and drain (S-D) contacts, to generate compressive (tensile) channel stress, or by the use of nitride layers as a gate stressor [28]. The detailed shape of active regions, polygates, and S-D contacts may have an impact on the way stress is distributed inside the chip, from chip-to-chip, over the wafer. Also, well-known CMP planarization, and subsequent dielectric deposition, will add shape-dependent stress.

These effects need to be fully understood to minimize their potential impact. Then, they will have to be systematically tracked in order to monitor their variation from run-to-run, in such a way that the associated models and parameters follow the real performance of the fabrication process. This implies that the mass of information extracted will need appropriate statistical methodologies to understand the phenomena, and react in real-time.

IV. CHARACTERIZATION AND TEST STRUCTURES

To ensure future success, every process step will need to be critically analysed for potential variability, such as thermal non-uniformity during dopant activation, or local gas concentration variations, etc. But, some ramdom variabilities are intrinsic, and, indeed, already predicted. Such is the case for dopant atoms in the channel, or for variations in actual channel length due to line roughness, which, coupled with short-channel effects, produces V_{th} dispersion leading to complete noise-margin loss.

Purely static evaluation of variabilities is not enough since their effects could also manifest themselves in frequency and/or in time. New dielectrics, for example, could present this behavior, and it is imperative to know their whole spectrum of responses, since some applications, or their reliability, could be affected. Moreover, conductive layers may be affected by electro-migration or even by skin-depth effects at high frequencies.

Thus, realistic design-based test structures can play a key role in extracting significant data, and adequate models leading to optimum Global Design. Current Design for Manufacturing (DfM) allows some yield improvement in spite of process variabilities through the use of statistical techniques [29], but its scope is limited by our lack of knowledge of the intrinsic physical phenomena at the heart of the source of variability.

The number and complexity of devices necessary to capture device and process behavior, has been steadily increasing for recent technology nodes, reflecting the fact that simple scribe-line devices are insufficient, since, now, detailed assessment of Within-the-Die (WiD) variation monitoring is mandatory. In addition, stray- coupling effects have also become more important, as mentioned, in correlation with different design styles and chip/device orientations. In order to be useful, the data cited above needs to be statistically significant, which implies a steep growth in the number of test-focussed devices and in the associated data processing. Thus, the measurement effort and associated modeling needs to be carefully taken into account in the choice of the test structures, since continuous monitoring of the process and of the circuit behavior is a must. Ideally, test times should remain on the order of *5 minutes/wafer*. A Test Structure Compiler has been proposed by IBM [30] to reduce the burden posed by the design of these structures and lower the entry barrier. Ideally, this will reduce the time needed to introduce new structures, bringing some standardization to this domain, which is portable with respect to future technology-node change.

Because of the tight coupling between three factors - the way a chip is organized and laid out, the device architecture, and the effect of all the different process steps - a close interaction between System/Circuit/Device/Process design, is necessary from the very early stages, since detailed modeling and interpretation is needed at all these levels. Potentially, multi-dimensional modeling will contribute to the conversion of uncertainty to variability, as well as reduction in excessive margins and general pessimism (eg, corners).

V. THE MASTAR SIMULATION TOOL AND MODELING.

a) Model-Based DFM

One of the problems to be solved at the early stage is the generation of accurate physically-based electrical models, ones capable of incorporating various expected sources of variability. Such models would then need to be characterized and calibrated against data coming from either hard experiment from other physical or TCAD models (including local OPC effects) when hard data is not yet available. Thus, TCAD will contribute layout considerations to device spatial variability.

Then, such a model can be coupled to a SPICE-like circuit simulator to provide first estimations of typical-circuit block behavior.

b) Statistical Variations and Models

MASTAR [31] is a pre-SPICE model generator especially conceived for the calculation of the electrical characteristics of advanced CMOS transistors based on various technologies, such as planar-bulk, Double-Gate (DG), or Silicon-On-Insulator (SOI). Its calculations are based on analytical drift diffusion equations, which depend directly on the major technological parameters, such as gate length, channel doping, oxide thickness, etc. This model generator allows the user to evaluate, *immediately,* the impact of these technological parameters on the main transistor characteristics, such as the threshold behavior, performance values, or time delays. Moreover, the influence of secondary "physical" parameters such as mobility, poly depletion, and dark space, can be visualized, giving a deep insight into the physics of CMOS devices.

Currently, MASTAR plays a key role in device exploration, and process-module choice and optimization, through its ability to help predict realistic circuit behavior, in the same way that people refer to "virtual factories" in the literature [32]. Coupling MASTAR with appropriate test structures and associated statistical processing, with deep understanding and modeling of phenomena, and with details of the layout, will allow early estimation of the expected yield, and, thus, of the impact of individual design choices made at all levels.

VI. CIRCUIT TECHNIQUES

The traditional way to tackle component-variability problems has been to design in large error margins (corners) to ensure circuit functionality in the worst-possible cases. This excessively- pessimistic approach was the result of our inability to understand the sources of the observed variations. Regrettably, this lack of knowledge resulted in a waste of design resources. increasing the cost [30]. Only a close Technology-Design cooperation will lead to understanding and adequate-modeling the sources of the observed variability. Only such cooperation can provide a more realistic approach, leading to a more efficient Global-Design paradigm.

Circuit environmental effects (power-supply noise, electro-magnetic compatibility, etc) are not new, and are of a different nature. They can be handled directly by adequate design. But, on-chip stray coupling via the substrate will strongly depend, not only on the geometrical configuration, but also on the nature of the substrate itself, especially at high frequencies. At high frequencies, the real circuit is far more complex than the original schematic suggests, due to these added parasitic effects. In the analog domain, power-supply voltage reduction, coupled with the difficulty of keeping a V_{dd} to V_t ratio of about 5 (because of the increased leakage currents) brings two options to consideration: One of these is to stop V_{dd} scaling, as is being suggested, with the consequent increased process modifications. The other, perhaps consider the more intensive, is the use of sampled-data signal processing, combined with digital signal processing, for frequencies up to around 5GHz. Other concurrent approaches include:

a) Regular Layout

The principle of regular layout is another response to process variability. Assuming that transistors with identical schematics but different layouts here lead to different electrical behaviors, introducing regularity in layout is an attractive way to address the root causes of the problem rather than taking complex engineering steps (such as, OPC, DFM, etc…) to limit their consequences.

Potentially by exploring different layout techniques, we can overcome most of the nano-effects which lower the average performance of logic blocks, because simulation can no longer be safely correlated with silicon measurements. Through deep understanding of the fabrication process, lithography, etching, chemical & mechanical polishing, and reticle enhancement, we can reverse-engineer the way we draw logic functions, and come up with a new optimized layout implementation. Presumably, in this way, we can return to having confidence that our current CAD tools and models now act as they did in older technologies.

Figure 1.3.5 and Fig. 1.3.6 give an example of a standard flip-flop drawn with classical and regular layouts, respectively. A few technical comments regarding layout regularity can be mentioned:

- STI Stress: This well-known submicron effect, discovered in 0.18µm technology, impacts transistor performance depending on gate-to-active-border distance. The regular layout of active shapes significantly limits the STI stress.

- Well-Proximity Effects: The phenomenon, identified and described in 90nm technology, impacts transistor performance depending on gate-to-well distances. The regular layout of active shapes can significantly limit its effect.

- Transistor Printing: This refers to the way drawn shapes are physically translated onto silicon, thereby impacting their actual electrical dimensions (transistor width and length). This effect can be reduced by increasing the spacing between edges or end-caps. However, a systematic layout approach that limits notches and jogs is far better to ensure that electrical dimensions are as close as possible to drawn sizings. In addition, density of critical layers is also impacting the actual sizes of those shapes, even of ones drawn regularly. For instance, poly lines drawn at fixed pitch, even if not actually used, are the best guarantee of stable gate length over the block, leading to very controlled transistor characteristics.

At a first glance, layout regularity leads to lower density, as elementary functions might need a larger area for their implementation. However, this is deceiving, since the gain in terms of simulation accuracy and smaller within-die and within-wafer process variability, translates into an SoC implementation with less design margin, absorbing most of the area penalty. In addition, the layout regularity relaxes some of the technology and manufacturing constraints, giving higher yield, and lower power consumption, as well as earlier product introduction.

b) Body-Biasing

Also, local parametric feedback can be used to compensate for threshold-voltage variation through the use of back-gating coupled with appropriate local sensors, at the cost of some added circuit overhead [33]. Similar techniques are well-known and have been used for low-power design.

c) SRAM; Functionality and SNM

SRAM bit cells are particularly sensitive to process variations that make the compromise between write-ability, stability, and full functionality, more difficult to reach. SRAMs, like all analog circuits, remain a difficult case to scale, and, like all digital circuits, must yield, with several million cell instances per chip. The

extreme need for optimization of SRAM cells requires dedicated statistical simulations, and design techniques able to predict the yield versus process variations. Statistical simulations based on improved Monte-Carlo or analytical methods can detect probabilities of failure for the SNM, write margin, or any of the cell metrics, with high accuracy, while new design techniques based on variable power supplies will tend to widen margins within these metrics [30].

However, the continuous scaling roadmap progressively reduces the functional window size, as shown in Fig. 1.3.7. In particular, application requirements impose technical specifications in complete opposition to device physics (that is, reduced leakage, stable V_{DD}, lower V_t, etc.). To overcome this difficulty, significant changes in the device architecture are envisioned. The traditional Bulk approach induces very wide spreads on the SRAM characteristics that will not be compensated by design techniques with the coming technologies. As shown in Fig. 1.3.8, new transistor architectures, with fewer mismatches will become mandatory to design functional 6T SRAMs under the conditions required by the applications.

In this example, the SNM, which represents the SRAM read-margin evaluation, achieves better control with Silicon-on-Nothing transistors than on Bulk, with SOI as an intermediate step.

System design should be involved, as well, to improve circuit reliability. Repair techniques, such as redundancy and Error-Code Correction can be widely used to recover single-bit errors due to variability. For instance, ECC can "hide" close to 100 errors per Megabit, with fewer than 100ppm failing chips left un-recovered.

VII. CONCLUSION

A detailed presentation of the new methodologies to be applied in order to close the loop between System Design, Circuit Design, Device Design, and Process Design (and vice-versa) has been described. It points toward at a truly new culture based on a Generalized Design-for-Manufacturability concept, with the final goal of Yield Maximization.

The proliferation of devices with each technology node increases the importance of concurrent engineering techniques to generate design parameters and libraries, at the same time as the process development takes place, all in the context of ever-present increasing variabilities and resulting challenges.

In this nano-cosmology, Generalized Design-for-Manufacturability (including current DfM, MfD, DfY, …DfX) will touch all of the above-mentioned dimensions in a new space where all of them are inter-dependent through process of a tightly-coupled Physical-Electrical-Mechanical-Process modeling. Such complete modeling will allow early detection of the impact of Design Choices at all levels, including manufacturing-equipment-related ones.

Still, CMOS will, for some time, remain the most powerful and industrially-viable device for System Integration, and exploiting its huge potential will require exponentially-growing investments, only affordable in the long-run through innovative Cooperation-with-Competition schemes. An example of these Collaborative- Development Efforts is the Crolles2 Alliance, initiated by Freescale, Philips, and STMicroelectronics, in a joint R&D and manufacturing effort directed toward the most-advanced industrial CMOS technologies, in a unique ***"Coopetition"*** model. In this model, R&D and Manufacturing share the same facilities and equipment, eliminating technology transfer, strongly absorbing fixed costs, and bringing R&D to the required level in the yield learing curve, accelerating process stabilization. Other contributions/collaborations involving Academia are also essential for early success.

The loop of interaction between process, design, and product, will continue to intensify (DfM, DfT, TfM… DfX). Circuit techniques will evolve toward Regular Layout, dynamically, self-adjusting circuitry, Statistical Static Timing Analysis (SSTA), Permanent IP tracking, etc. [35].

Design-skilled IDMs will be well prepared to manage this 4D interaction, since IDMs have all the actors "under the same roof", and thus will have a much shorter reaction time in meeting the market's seasonal cycles, with much shorter "Time to Yield".

This presentation has clearly shown the advantages of a tight coupling between Process, Circuit, Architecture, and System Design, at the very early stages, when the critical choices are made, thus creating a 4D knowledge continuum reminiscent of the ideas of General Relativity, extremely rich in consequences for the future of nano-electronics. This global view will be the key to our industry's survival, as we race through the last stages of device scaling.

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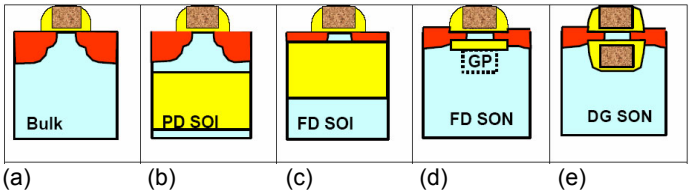

Figure 1.3.1: Possible device-structure chain as proposed at the Crolles-Alliance: (a)-Bulk, (b)-partially-depleted SOI, (c)-fully-depleted SOI, (d)-fully-depleted SON (Silicon-On-Nothing), (e)-double-gate SON.

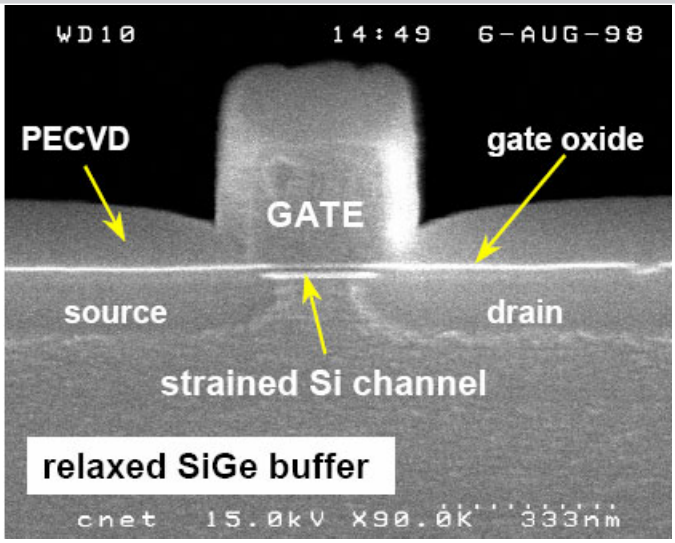

Figure 1.3.2: SEM photo of a MOS transistor with strained-Si channel. For more detail see [19].

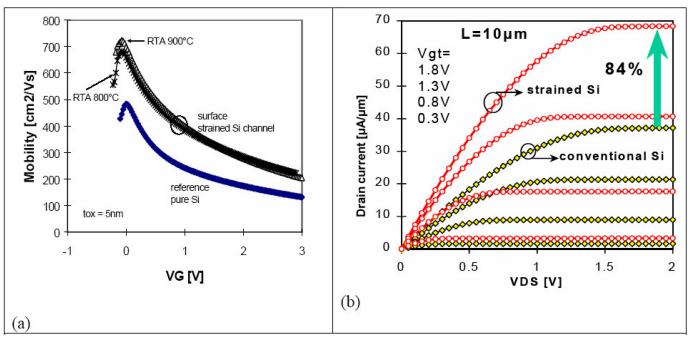

Figure 1.3.3: Comparison of (a) electron mobility between conventional Silicon- and strained- Silicon-channel transistors –, and (b) their output characteristics – Data taken from [19].

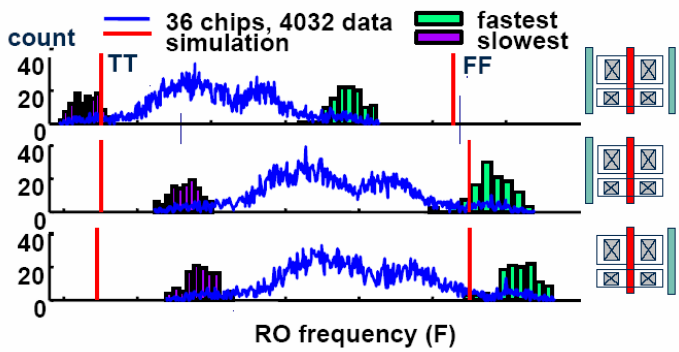

Figure 1.3.4: Effect of dummy poly lines on t_{pd} of ring oscillators [27].

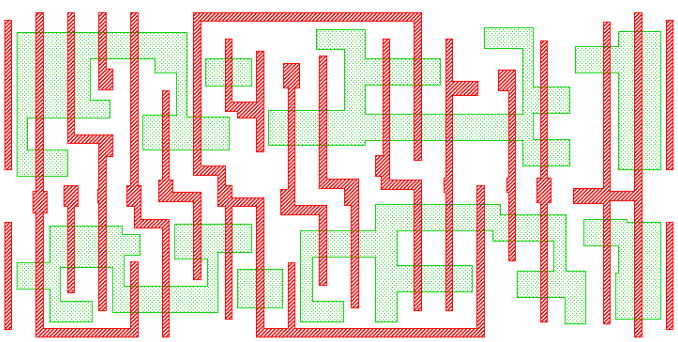

Figure 1.3.5: A standard flip-flop drawn using a classical layout approach.

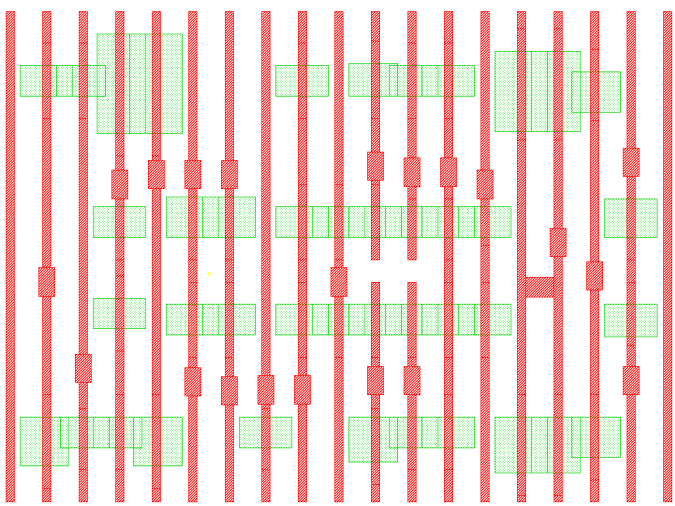

Figure 1.3.6 : The flip-flop of Figure 1.3.5 regular-layout implementation.

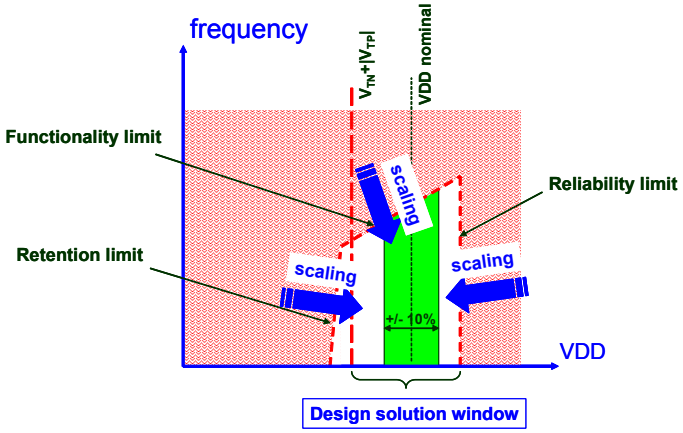

Figure 1.3.7: Functional window-size reduction induced by scaling.

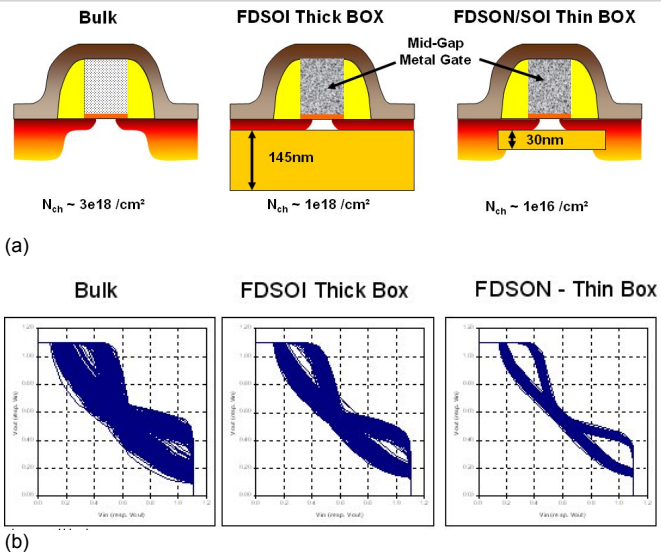

Figure 1.3.8: (a) SRAM devices and (b) MASTAR simulations [34].

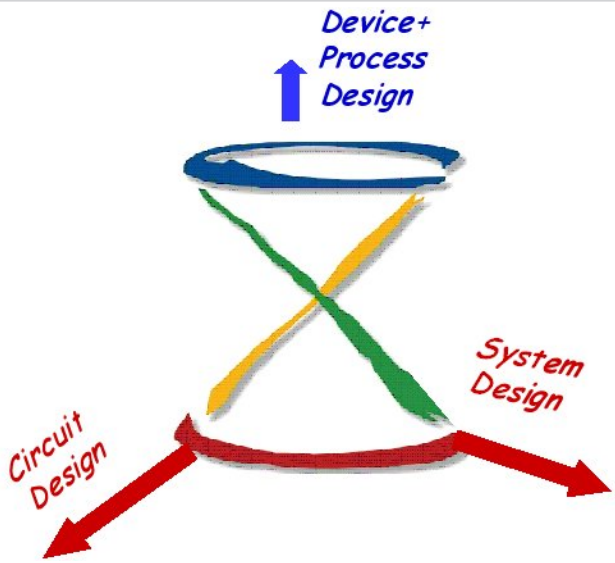

Figure 1.3.9: The 4D space of Generalized Design for Manufacturability.